REMARKS

The Office Action of November 30, 2005 was received and reviewed. Applicants would like to thank the Examiner for thorough review and consideration given to the above-identified application, and for indicating claims 7 and 9 as containing allowable subject matter and would be allowed if §112, 2nd paragraph rejection is overcome.

Claims 1-10 were pending prior to the instant amendment, of which claims 1, 7 and 9 are independent.

In the detailed Office Action, the title of the invention stands objected to, as the Examiner asserted that the title is still not sufficiently descriptive and that the title is not describing an invention that is neither clearly shown nor disclosed with respect to how VBB can be generated having a third potential lower than the second potential. In response, Applicants have replace the current title with a new title as shown above, which is deemed to be in accordance with MPEP §606 and 37 CFR 1.72(a). According to the MPEP, page 600-74, it is stated that the title of the invention should be brief but technically descriptive, preferably from two to seven words. It may not contain more than 500 characters. If the Examiner still asserts the title must show the low level details, such as a circuit having two transistors having a thicker gate oxides than two other transistors within a level shift circuit, Applicants would respectfully request the Examiner to point to an authority for such a requirement.

The abstract of the disclosure is still objected to because, like the title, the abstract is believed to be describing a substrate voltage generating circuit that is not clearly shown or disclosed, with respect to being able to generate voltage VBB. Further, the Examiner asserted that the output signal VBB cannot have a third potential while specifying that the output signal can have a first and a third potential, as disclosed in the abstract of the disclosure. Still further, the Examiner is not clear whether what is meant in the phrase "in response to the output signal VBB" on line 10 of the abstract. Still further, the specification stand objected to as the Examiner is unclear how substrate VBB is transferred to output node OUT.vbb as described on page 13, lines 14-17 of the specification, and where does VBB actually come from.

In response to the objection to the specification and abstract, Applicants respectfully note that the level shift circuit outputs VDD (i.e., a first potential) and VBB (i.e., third

potential level), as shown in Fig. 1 with the level shift circuit 101 and 102. The output signal of the level shift circuits 101 and 102 is inverted and input into the gate of SW1 and SW2. OUT.vbb, however, outputs VBB. In this regard, Applicants respectfully assert that the specification as well as the abstract contains no unclear language as asserted by the Examiner.

With respect to how VBB is generated, Applicants respectfully invite the Examiner to study the description of how the presently claimed invention operates in generating VBB (i.e., V_{BB}) in reference to the first power supply voltage VDD (i.e., V_{DD}) and second power supply voltage VSS (i.e., V_{SS}). For example, beginning on page 11, line 8, the description of how the operation of the substrate voltage generating circuit according to a first embodiment, as shown in Figs. 1 and 2, is discussed. In another example, starting on page 18, line 13, the description of how the presently claimed invention according to a second embodiment, as shown in Figs. 1 and 3, is discussed.

As shown in Fig. 1, for example, the potential level inputs and outputs of each component are clearly shown. For example, NAND 1 can have either VDD or VSS as an output voltage level, output out.101 of level shift circuit 101 can have either VDD or VBB as an output voltage level, and so on. Hence, the behavior of each element in response to a certain input is clearly shown from the input signal OSC, /OSC and pump, power supply input VDD and VSS, to the final output signal OUT.vbb with substrate voltage VBB (i.e., V_{BB}).

Applicants note that the output substrate voltage VBB generated is also used as an input to the source of the 5^{th} and 6^{th} transistors N3 and N4, respectively, in Fig. 2. Also, VBB is used as an input voltage at the source of the 5^{th} and 6^{th} transistors N33 and N34, respectively, as shown in Fig. 3. This feedback of the generated VBB substrate voltage, although not explicitly described in the specification, is clearly shown in Fig. 1 with a connection of OUT.vbb to level shift circuits 101 and 102. Further, VBB at OUT.vbb is generated by making the voltage of capacitor C1 or C2 descend from VSS. Additionally, SW1 and SW2 are switched on alternately. Thus, pulled down voltage VBB is applied to the output node OUT.vbb before the voltage at the output node becoming VSS.

It appears that the Examiner assumed that OUT.vbb would be pulled down to VSS (ground). This assumption requires that SW1 or SW2 be switched on and stay on for a

period of time until a steady state of 0V is reached at OUT.vbb. However, this assumption is not accurate, as SW1 and SW2 switch on alternately and cooperate via feedback with the rest of the level shifting circuits to produce VBB and not VSS. In view of the response set forth above, the objection to the specification and abstract is respectfully requested to be reconsidered and withdrawn.

Claims 1-6 remain rejected under 35 U.S.C. §112, first paragraph, as the Examiner asserted that the specification, while being enabling for a level shift circuit, does not reasonably provide enablement for a substrate voltage generating circuit, and that the use of "substrate voltage generating circuit" in the preamble of claim 1 does not accurately identify the circuit being described in the claim. In response, Applicants respectfully submit that claims 1-6 are of varying scopes, with claim 1 being the broadest. That is, claims 1-6 are directed to the broadest invention of a substrate voltage generating circuit, with claims 2 and 3 further narrowing the scope by further reciting the details of the level shift circuit of claim 1. Hence, the language in the preamble of claim 1 is proper.

As the Examiner requires detailed explanation of how VBB is generated, Applicants have complied herein by providing additional explanation above to supplement in previously submitted explanation in the Amendment filed September 12, 2005 which is incorporated herein by reference. Accordingly, the §112, 1s paragraph rejection is respectfully requested to be reconsidered and withdrawn.

Claims 1-10 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. In this rejection, the Examiner appears to assume again that the output node would be at the second voltage potential (i.e., VSS) and not at the third voltage potential (i.e., VBB) when SW1 or SW2 are switched on. As noted above, this assumption is not accurate, as SW1 and SW2 switch on alternately and cooperate via feedback with the rest of the level shifting circuits to produce VBB and not VSS.

With respect to the Examiner's confusion between "an input signal having the first and second potential levels" in claim 1 and the use of "the input signal" in claim 2, Applicants note that the features of claim 2 are supported by Fig. 2. As explained in the previously submitted Amendment, the input signal having the first and second potential levels correspond to VDD and VSS, respectively. In Fig. 1, the input signal are inputted into

in.101 of first transistor P1 and /in.101 of second transistor P2. The input signal may take a potential level of H or L (i.e., VDD or VSS, respectively). That is, the input signal to the first transistor P1 is complementary to the input signal transistor P2 as shown in Fig. 2, and the input signal to level shift circuit 101 shown in Fig. 1 are from the output of NAND1 is shown as DSS/VSS and INV 7 as VDD/VSS. Hence, there is no confusion between "an input signal having the first and second potential levels" in claim 1 and the use of "the input signal" in claim 2 as alleged by the Examiner.

With respect to the Examiner's allegation that claim 3 has the same problem as claim 2, Applicants note that the features of claim 3 are supported by Fig. 3, for example. Applicants' clarification of the claim language in claim 2 above and the response to the §112, 2nd paragraph rejection in the Amendment filed September 12, 2005 are also applicable to claim 3. The language "the input signal" directed to the first transistor and the second transistor in claim 3 means that the input signal to the first transistor P31 or to the second transistor P32 may be VDD or VSS (i.e., first and second potential levels, respectively). Due to the complementary nature of the input signal to the first transistor P31 and to second transistor P32, wherein the input signal's may be of VDD and VSS potential level (i.e., first potential level is High and second potential level is Low) as indicated in claim 1, the language "the input signal" in claim 3 is intended to cover the changing nature of the input signal and is deemed as sufficiently clear. Should the Examiner is still confused by the claim language, Applicants would respectfully consider further clarifying the language so that the pending §112, 1st and 2nd rejections will be overcome and the claims be allowed.

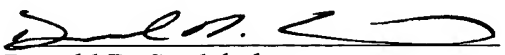
With respect to independent claims 7 and 9, which are objected to, Applicants respectfully assert that the responses in relation to claims 1-3 set forth above in relation to the pending §112, 1st and 2nd rejections are also applicable.

In addition to the arguments set forth above, Applicants respectfully submit that the presently claimed invention is directed to a substrate generating circuit having a level shift circuit and providing a third potential (VBB) level at an output node, as recited in claim 1 which is the broadest claim in the group of claims 1-6. The claimed invention is further narrowed in scope by the additional recital of the structural and functional details of the level shift circuit in dependent claims 2-6, for example.

Cases have held that "if a claim adequately defines patentable subject matter and meets the disclosure and clarity standards of Section 112, then it is proper, even though it may encompass less than what the invention could claim." *Andrew Corp. v. Gabriel Electronics, Inc.* (Fed. Cir. 1988). Further, Applicants respectfully direct the Examiner to MPEP §2164.08 (page 2100-191, Rev. 1, Feb. 2003). It is stated therein that when analyzing the enabled scope of a claim, the teaching in the specification must not be ignored because claims are to be given their broadest reasonable interpretation that is consistent with the specification, and that claims are interpreted in light of the specification does not mean that everything in the specification must be read into the claims. Moreover, according to MPEP 608.01(m), claims should be arranged in order of scope so that the first claim presented is the least restrictive. Keeping in mind of the guideline from the MPEP and legal precedents noted above, Applicants note that claims 1-6 are of varying scope, as Applicants' are entitled to claiming, and that independent claim 1 and its dependent claims 2-6 do not stand or fall together. Similarly, independent claims 7 and 9 do not stand or fall together with their respective dependent claims 8 and 10.

In view of the foregoing, it is respectfully requested that the rejections and objection of record be reconsidered and withdrawn by the Examiner, that claims 1-10 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



Donald R. Studebaker
Registration No. 32,815

NIXON PEABODY LLP
Suite 900, 401 9th Street, N.W.
Washington, D.C. 20004-2128
(202) 585-8000